REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1 and 2 are pending in the present application. Claims 1 and 2 have been amended by the present amendment without introducing new matter.

In the outstanding Office Action, Claim 1 was objected to; Claim 1 was rejected under 35 U.S.C. § 102(b) as anticipated by Chen (U.S. Patent 6,313,003); and Claim 2 was rejected under 35 U.S.C. § 103(a) as unpatentable over Chen in view of Brabazon et al. (U.S. Patent 6,008,083, herein "Brabazon").

First, Applicants respectfully request the Examiner to clarify whether the drawings filed June 30, 2003 are accepted or objected.

A new abstract that better reflects the claimed invention is presented.

With regard to the objection to Claim 1, Claim 1 has been amended in light of the comments noted in the outstanding Office Action. Accordingly, it is respectfully requested this objection be withdrawn.

Claims 1 and 2 have been amended to better reflect the claimed invention, and to better correspond to U.S. claim drafting practice. Further, amended Claims 1 and 2 find support in the specification as originally filed. No new matter is added.

Claim 1 stands rejected under 35 U.S.C. § 102(b) as anticipated by Chen. This rejection is respectfully traversed.

Amended Claim 1 is directed to a method of manufacturing a semiconductor device including (a) forming a first interlayer insulation film on a semiconductor substrate, (b) depositing a first metal film on the first interlayer insulation film, (c) depositing an antireflection film including a dielectric layer on an upper surface of the first metal film, (d) patterning the first metal film and the antireflection film to form a lower electrode having the

antireflection film on an upper surface thereof, (e) forming a second interlayer insulation film on the antireflection film, (f) forming first and second openings in a first region and in a second region in the second interlayer insulation film, respectively, (g) removing a portion of the antireflection film where the second opening is formed, (h) depositing a second metal film on the second interlayer insulation film, and (i) removing the second metal film except in the first and second openings to form an upper electrode in the first opening, and a contact in the second opening.

In a non-limiting example, Figures 1-4 illustrate (a) forming a first interlayer insulation film 1 on a semiconductor substrate, (b) depositing a first metal film 3 on the first interlayer insulation film 1, (c) depositing an antireflection film 4 including a dielectric layer 42 on an upper surface of the first metal film 3, (d) patterning the first metal film 3 and the antireflection film 4 to form a lower electrode having the antireflection film 4 on an upper surface thereof, (e) forming a second interlayer insulation film 5 on the antireflection film 4, (f) forming first and second openings (51, 52) in a first region and in a second region in the second interlayer insulation film 5, respectively, (g) removing a portion of the antireflection film 4 where the second opening 52 is formed, (h) depositing a second metal film 8 on the second interlayer insulation film 5, and (i) removing the second metal film 8 except in the first and second openings (51, 52) to form an upper electrode 81 in the first opening 51, and a contact 82 in the second opening 52.

Chen discloses depositing of a layer 54 of insulation on the surface of a substrate 10 provided with points of electrical contact (48, 50, 52), depositing of a layer 56 of dielectric on the layer 54, forming of an opening 58 by etching the layers (54, 56), depositing of a layer 60 of insulation, forming of openings (62, 64) by etching the layers (54, 56, 60), and filling the openings (58, 62, 64) with metal to form plugs (66, 68, 70) (see column 7, line 66 to, column 10, line 32, and Figures 3-6). However, Chen does not disclose or suggest all of the claimed

features. Specifically, Chen does not disclose or suggest "(a) forming a first interlayer insulation film on a semiconductor substrate, (b) depositing a first metal film on said first interlayer insulation film, (c) depositing an antireflection film including a dielectric layer on an upper surface of said first metal film, (d) patterning said first metal film and said antireflection film to form a lower electrode having said antireflection film on an upper surface thereof ..." as recited in amended Claim 1.

Accordingly, it is respectfully submitted that independent Claim 1 and each of the claims depending therefrom define over Chen.

Claim 2 stands rejected under 35 U.S.C. § 103(a) as unpatentable over Chen and Brabazon. This rejection is respectfully traversed.

Claim 2 depends on Claim 1, which as discussed above defines over Chen. Further, Brabazon also does not disclose or suggest all of the features recited in amended Claim 1.

Because neither Chen nor Brabazon discloses or suggests all of the features recited in amended Claim 1, the combined teachings of the references do not render obvious the method of manufacturing a semiconductor device as recited in amended Claim 1.

Accordingly, it is respectfully requested this rejection be withdrawn.

Consequently, in light of the above discussion, and in view of the present amendment, Applicants respectfully submit that the present application is in condition for allowance, and an early action favorable to that effect is earnestly solicited.

Respectfully submitted,

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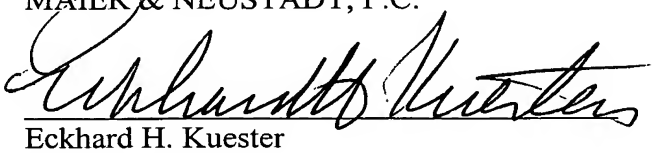

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